

BEST AVAILABLE COPY**REMARKS**

Applicant thanks the Examiner for the thorough examination of the application. The FINAL Office Action, however, has maintained its rejections to all pending claims 16-63. Applicant continues to disagree with the rejections for all applicable reasons, which were advanced in last response. As it appears this application is headed for appeal, Applicant sets forth the following additional comments for consideration, as well as to set up these issues for appeal.

Present Status of Application

Claims 16-24, 26-36, 38-46, 48-57, and 59-63 are rejected under 35 U.S.C. 102(b) as allegedly anticipated by U.S. Patent No. 5,278,438 to Kim et al. Claims 25, 37, 47, and 58 are rejected under 35 U.S.C. 103(a) as allegedly unpatentable by U.S. Patent No. 5,278,438. Claims 25, 37, 47, and 58 are rejected under 35 U.S.C. 103(a) as allegedly unpatentable over U.S. Patent No. 5,278,438. Finally, claims 16, 28, 39, and 50 are rejected under 35 U.S.C. 103(a) as allegedly unpatentable by U.S. Patent No. 5,851,881 to Lin et al, in view of Mendicino, Patent No. 6,271,143. For at least the additional reasons set forth herein (in addition to those advanced in Applicant's previous response), Applicant requests reconsideration and withdrawal of the rejections.

Rejections Under 35 U.S.C. 102(b)

Claims 16-24, 26-36, 38-46, 48-57, and 59-63 are rejected under 35 U.S.C. 102(b) as allegedly anticipated by U.S. Patent No. 5,278,438 to Kim et al.

Claim 16 recites:

16. A method of fabricating a self-aligned conductive region to active region structure comprising:
providing a semiconductor region within a substrate extending to a surface,

forming a gate insulator layer over said semiconductor region;

forming, sequentially, a conductive layer, an insulator layer and a hard mask layer over said gate insulator layer;

patterning said gate insulator layer, said conductive layer, said insulator layer and said hard mask layer to form a plurality of tiered parallel stripes;

forming a spacer insulator layer over the sidewalls of said parallel stripes;

forming trenches in said semiconductor region between said parallel stripes;

growing an insulator liner layer over sides of said trenches, and depositing an insulator filler layer so that said trenches and the space between said parallel stripes are filled with said insulator filler layer;

planarizing so that said insulator filler layer above top of said insulator layer is removed and said hard mask is removed;

etching said filler layer so that it just fills said trenches;

removing said insulator layer and said insulator spacer layer; and

patterning said conductive layer to form separated conductive regions.

(Emphasis Added). Applicant submits that independent claim 16 patentably defines over the cited art for at least the reason that the cited art fails to disclose the features emphasized above.

It is clear that the claimed method of fabricating a self-aligned conductive region to active region structure in claim 16 comprises *removing said insulator layer and said insulator spacer layer*. The Office Action alleges that "Kim teaches removing said insulator layer and said insulator spacer layer, and patterning said conductive layer to form separated conductive regions in Col. 5, lines 28-46, and figs. 1-6, 13"

However, and referring to 5, lines 28-46, Figs. 1-6, 13, Kim teaches:

After completion of the source and drain implantation, the trench is filled in with oxide and planarized to expose the nitride layer 19. Using the initial LOCOS oxide stripes 11 as an etch stop, the column of stacked poly gate structure 12 is etched to isolate independent stacked poly gate cells 20 as shown in FIG 13. The etching exposes sides 27 of the stacked poly gate cells 20. The exposed sides 27 can be passivated by a thermal oxidation method to form protective oxide on the exposed sides while the nitride layer 19 keeps the poly surface of the cell 20 from oxidation.

As can be readily verified from the foregoing, it is clear that Kim teaches that the column of stacked poly gate structure 12 is etched to isolate independent stacked poly gate cells 20 subsequent to the steps of FIG 5, in which the insulator 19 or the spacers 26 and 28 are not removed. Even FIG 13 does not show the

spacers, FIG 13, however, is only a sketch map, which cannot indicate that Kim teaches removing the spacers for the following reasons. If the spacer taught by Kim is removed, sidewalls of the stacked poly gate cells 20 and the sidewalls of the trenches 30 or 42 are not continuous. Consequently, Kim indeed does not disclose "removing said insulator layer and said insulator spacer layer," as expressly recited in claim 16.

MPEP 2131 states:

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "When a claim covers several structures or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art." *Brown v. 3M*, 265 F.3d 1349, 1351, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) (claim to a system for setting a computer clock to an offset time to address the Year 2000 (Y2K) problem, applicable to records with year date data in "at least one of two-digit, three-digit, or four-digit" representations, was held anticipated by a system that offsets year dates in only two-digit formats). See also MPEP § 2131.02. < *The identical invention must be shown in as complete detail as is contained in the ... claim.*" *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Note that, in some circumstances, it is permissible to use multiple references in a 35 U.S.C. 102 rejection. See MPEP § 2131.01.

It is clear that not every element, as specifically set forth in the claim 16, is found in Kim.

Consequently, the cited reference fails to anticipate claim 16, as allegedly by the Office Action. For at least this additional reason, reconsideration of this rejection is hereby respectfully requested.

For similar reasons, independent claims 28, 39, and 50 are also patentable.

Rejections Under 35 U.S.C. 103(a)

Claims 25, 37, 47, and 58 are rejected under 35 U.S.C. 103(a) as allegedly unpatentable by U.S. Patent No. 5,278,438. Claims 25, 37, 47, and 58 are rejected under 35 U.S.C. 103(a) as allegedly unpatentable over U.S. Patent No. 5,278,438. Claims 16, 28, 39 and 50 are rejected under 35 U.S.C. 103(a)

as allegedly unpatentable by U.S. Patent No. 5,851,881 to Lin et al, in view of Mendicino, Patent No. 6,271,143.

Independent claim 16 recites:

16. A method of fabricating a self-aligned conductive region to active region structure comprising:
providing a semiconductor region within a substrate extending to a surface, forming a gate insulator layer over said semiconductor region;
forming, sequentially, a conductive layer, an insulator layer and a hard mask layer over said gate insulator layer;
patterning said gate insulator layer, said conductive layer, said insulator layer and said hard mask layer to form a plurality of tiered parallel stripes;
forming a spacer insulator layer over the sidewalls of said parallel stripes;
forming trenches in said semiconductor region between said parallel stripes;
growing an insulator liner layer over sides of said trenches, and depositing an insulator filler layer so that said trenches and the space between said parallel stripes are filled with said insulator filler layer;
planarizing so that said insulator filler layer above top of said insulator layer is removed and said hard mask is removed;
etching said filler layer so that it just fills said trenches;
removing said insulator layer and said insulator spacer layer; and
patterning said conductive layer to form separated conductive regions.

(Emphasis added.)

Applicant respectfully submits that the step of patterning said conductive layer to form separated conductive regions in claim 16 is not disclosed by Lin. In addition, Mendicino also fails to teach this feature.

MPEP 2142 provides, in part:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. *Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In connection with the third criteria, MPEP 2143.03 goes on the state:

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Applicant therefore submits that, even when taken in combination, Lin and Mendicino fail to teach or suggest all of the limitations recited in claim 16. For at least this reason, claim 16 is allowable over the cited reference. Reconsideration of this rejection is hereby respectfully requested.

As a separate and independent basis for the patentability of claim 16, Applicants respectfully traverse the rejections as failing to identify a proper basis for combining the cited references. In combining these references, the Office Action stated only that the combination would have been obvious "in order to reduce or prevent the trench fill erosion, thereby eliminating or reducing the adverse device affects of the parasitic sidewall." (Office Action, page 9). This alleged motivation is clearly improper in view of well-established Federal Circuit precedent.

It is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103, there must have been some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious. *W. L. Gore & Associates, Inc. v. Garlock* Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

"The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. . . ." Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(*Emphasis added.*) In re Dow Chemical Company, 837 F.2d 469, 473 (Fed. Cir. 1988).

In this regard, Applicants note that there must not only be a suggestion to combine the functional or operational aspects of the combined references, but that the Federal Circuit also requires the prior art to suggest both the combination of elements and the structure resulting from the combination. Stiftung v. Renishaw PLC, 945 Fed.2d 1173 (Fed. Cir. 1991). Therefore, in order to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements to derive a method of forming a self-aligned floating gate, as claimed by the Applicants.

When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. Gambro Lundia AB v. Baxter Healthcare Corp., 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997) (also noting that the "absence of such a suggestion to combine is dispositive in an obviousness determination").

Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. See In re Dembiczkak, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be "clear and particular." Dembiczkak, 175 F.3d at 999, 50 USPQ2d at 1617.

If there was no motivation or suggestion to combine selective teachings from multiple prior art references, one of ordinary skill in the art would not have viewed the present invention as obvious. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998);

Gambro Lundia AB, 110 F.3d at 1579, 42 USPQ2d at 1383 ("The absence of such a suggestion to combine is dispositive in an obviousness determination.").

Significantly, where there is no apparent disadvantage present in a particular prior art reference, then generally there can be no motivation to combine the teaching of another reference with the particular prior art reference. Winner Int'l Royalty Corp. v. Wang, No 98-1553 (Fed. Cir. January 27, 2000).

For at least the additional reason that the Office Action failed to identify proper motivations or suggestions for combining the various references to properly support the rejection of claim 16 under 35 U.S.C. § 103, that rejection should be withdrawn.

For similar reasons, independent claims 28, 39 and 50 are also patentable.

Claims 16, 28, 39 and 50 are independent claims, on which claims 17-27, 29-38, 40-49 and 51-59 respectively depend. Applicant asserts that claim 16, 28, 39 and 50 are patentable for the reasons discussed, and therefore for at least the same reasons, claims 17-27, 29-38, 40-49 and 51-59 are patentable.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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